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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,262	02/07/2002	Ian Bryant	ACT-318	9640

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

PR4

Office Action Summary	Application No.	Applicant(s)
	10/071,262	BRYANT ET AL.
	Examiner	**Art Unit**
	Cynthia Britt	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-6_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-6_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _20 May 2002_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _6,7_.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-6 are presented for examination.

Priority

The benefits of an earlier application (09/654240 filed September 2, 2000) have been noted. This application has issued and is now U.S. Patent No. 6,476,636, and should replace the application number in the first line of this application.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on April 29, 2002 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

The information disclosure statement (IDS) submitted on February 03, 2004 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The replacement formal drawings were received on May 20, 2002. These drawings are acceptable.

Specification

The abstract of the disclosure is objected to because it does not contain any reference to what is new in this continuation in part application (abstract is the same as

previous application). Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include *that which is new in the art to which the invention pertains*. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

(1) if a machine or apparatus, its organization and operation;

(2) if an article, its method of making;

(3) if a chemical compound, its identity and use;

(4) if a mixture, its ingredients;

(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2-6 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The terms "predicting an expected syndrome", "obtaining actual syndrome values", critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The term "syndrome" as used in the present specification and claims is unclear. There is no explanation in the specification as to how this syndrome is calculated or predicted. On page 6 of the specification line 11-13 states "The BIST syndrome is then calculated, generating actual values. The expected values are then compared with actual values." On page 11 of the present specification lines 20-21 refers to "a MISR syndrome capture unit". It is also unclear to the examiner what a BIST syndrome, or MISR syndrome is used to accomplish, and if these two are actually the same syndrome. The claims however only specify "actual" or expected" syndromes as discussed on pages 14 (lines 18-21) and 15 (lines 1-2) of the present specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal U.S. Patent No. 5,572,712 in view of Abramovici et al. U. S. Patent No. 6,550,030.

As per claims 1, Jamal substantially teaches the claimed method of developing circuit specifications including base specifications describing base functionality and BIST specifications describing BIST functionality. The base specifications are described in a hardware description language to create a base HDL, and the base HDL is input into a digital computer system. Utilizing both the base specifications and the BIST specifications, a BIST HDL is created on the digital computer system. A netlist is synthesized on the computer system from both the base HDL and the BIST HDL. Thereafter, a digital integrated circuit is produced as specified by the netlist. (Column 2 lines 1-11) Not explicitly disclosed is that this is used for FPGA circuitry.

However, in an analogous art, Abramovici et al. teach that a typical field programmable gate array (FPGA) generally consists of an array of programmable logic blocks interconnected by a programmable routing network and programmable input/output cells or boundary-scan ports (most FPGAs feature a boundary-scan mechanism). The programmable logic blocks of an FPGA are completely tested during normal operation. In order to test the programmable logic blocks during normal operation, the FPGA resources are configured into a working area and a self-testing area. The steps of configuring, testing, reconfiguring, and roving the resources of an FPGA under test are necessarily controlled by a test and reconfiguration controller. In the preferred embodiment, an external test and reconfiguration controller is utilized because present commercially available FPGAs do not allow internal access to their configuration memory. Accordingly, a configuration decompiler tool of a type known in the art is utilized to determine the intended function or mode of operation of the FPGA

resources. Alternatively, *this information may be extracted from the design stage and made available to the controller*. It should be appreciated by those skilled in the art that any controller, e.g., internal or external to the FPGA, could be utilized with an FPGA that allows for internal access to its configuration memory and that a single test and reconfiguration controller is capable of controlling several FPGAs (FIG. 1, column 4 lines 3-35). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of Jamal with the FPGA circuitry of Abramovici et al. This would have been obvious as suggested by Abramovici et al. (column 1 lines 48-55) in order to have integrated circuitry with reconfigurable hardware to be highly reliable and available.

As per claims 3-4 Abramovici et al. teach that the programmable logic blocks within the initial self-testing area are configured to include a test pattern generator (TPG), an output response analyzer (ORA), and equivalently configured programmable logic blocks (PLBs) under test. During testing, equivalent test patterns generated using the TPG are received by the PLBs under test. The outputs of the PLBs under test are compared by the ORA to determine whether a fault exists within either of the PLBs under test. A match/mismatch result of the comparison performed by the ORA is communicated as a pass/fail result or fault status data through the boundary-scan ports of the FPGA (not shown) to the controller. The fault status data is stored in memory and utilized by the controller in reconfiguring the PLB for fault tolerant operation. If an incremental routing job is unable to be completed, the original FPGA configuration is unable to implement roving and the netlist is rerouted after reserving several segments

in the congested area. (Column 5 lines10-30, column 9 line 60 through column 10 line 19, FIG. 4)

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhawmik et al. U. S. Patent No 6,463,560 in view of Abramovici et al. U. S. Patent No. 6,550,030.

As per claims 5 and 6, Bhawmik et al. substantially teach the claimed circuit and method for implementing a BIST scheme in an integrated circuit for testing RTL controller data paths in the integrated circuit, with the steps of: extracting a state table from a controller netlist of a controller circuit within the integrated circuit; selecting untested RTL elements from an RTL circuit in the integrated circuit; extracting test control and data flow (TCDF) information for the selected RTL elements from the extracted state table, controller netlist and a data path of the circuit; performing a symbolic testability analysis of the extracted test control and data flow information to derive a test environment; identifying a controller input sequence for the derived test environment; modifying an existing controller input sequence of the integrated circuit with the identified controller input sequence; synthesizing a BIST controller from the modified controller input sequence; and modifying the integrated circuit with a BIST architecture having the synthesized BIST controller and the controller input sequence for testing of the integrated circuit. (Column 21 line 44 through column 22 line 21) Not explicitly disclosed is that this is used for FPGA circuitry.

However, in an analogous art, Abramovici et al. teach that a typical field programmable gate array (FPGA) generally consists of an array of programmable logic blocks

interconnected by a programmable routing network and programmable input/output cells or boundary-scan ports (most FPGAs feature a boundary-scan mechanism). The programmable logic blocks of an FPGA are completely tested during normal operation. In order to test the programmable logic blocks during normal operation, the FPGA resources are configured into a working area and a self-testing area. The steps of configuring, testing, reconfiguring, and roving the resources of an FPGA under test are necessarily controlled by a test and reconfiguration controller. In the preferred embodiment, an external test and reconfiguration controller is utilized because present commercially available FPGAs do not allow internal access to their configuration memory. Accordingly, a configuration decompiler tool of a type known in the art is utilized to determine the intended function or mode of operation of the FPGA resources. Alternatively, *this information may be extracted from the design stage and made available to the controller*. It should be appreciated by those skilled in the art that any controller, e.g., internal or external to the FPGA, could be utilized with an FPGA that allows for internal access to its configuration memory and that a single test and reconfiguration controller is capable of controlling several FPGAs (FIG. 1, column 4 lines 3-35). The programmable logic blocks within the initial self-testing area are configured to include a test pattern generator (TPG), an output response analyzer (ORA), and equivalently configured programmable logic blocks (PLBs) under test. During testing, equivalent test patterns generated using the TPG are received by the PLBs under test. The outputs of the PLBs under test are compared by the ORA to determine whether a fault exists within either of the PLBs under test. A match/mismatch

result of the comparison performed by the ORA is communicated as a pass/fail result or fault status data through the boundary-scan ports of the FPGA (not shown) to the controller. The fault status data is stored in memory and utilized by the controller in reconfiguring the PLB for fault tolerant operation. If an incremental routing job is unable to be completed, the original FPGA configuration is unable to implement roving and the netlist is rerouted after reserving several segments in the congested area. (Column 5 lines10-30, column 9 line 60 through column 10 line 19, FIG. 4)

Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the method of Jamal with the FPGA circuitry of Abramovici et al. This would have been obvious as suggested by Abramovici et al. (column 1 lines 48-55) in order to have integrated circuitry with reconfigurable hardware to be highly reliable and available.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,631,487 Abramovici et al.

This patent teaches a method of testing field programmable gate array (FPGA) resources and identifying faulty FPGA resources during normal on-line operation includes configuring an FPGA into a working area and an initial self-testing area. The

working area maintains normal operation of the FPGA throughout testing and identifying of the resources. Within the initial and subsequent self-testing areas, the FPGA resources are initially tested for faults. Upon detection of a fault in the FPGA resources, the initial self-testing area resources are reconfigured or subdivided and further tested in order to identify the faulty resource. Dependent upon the further test results, the FPGA resources may be further subdivided and tested until the faulty resource is identified. Once the faulty resource is identified, the FPGA is reconfigured to replace unusable faulty resources or to avoid faulty modes of operation of partially faulty resources diagnosed during further testing.

U.S. Patent No. 6,681,354 Gupta

This patent teaches a field programmable gate array for use in an integrated processing system capable of testing other embedded circuit components in the integrated processing system. The field programmable gate array detects a trigger signal (such as a power reset) in the integrated processing system. In response to the trigger signal, the field programmable gate array receives first test program instructions from a first external source and executes the first test program instructions in order to test the other embedded circuit components in the integrated processing system. When testing of the other embedded circuit components is complete, the field programmable gate array loads its normal operating code and performs its normal functions.

U.S. Patent No. 6,301,688 Roy

This patent teaches a method for inserting test points in RTL VHDL designs or other high level circuit designs such that after a synthesis process the resulting gate-level design contains test points which improves fault coverage in a Full Scan BIST environment.

U.S. Patent No. 5,878,051 Sharma et al.

This patent teaches an assembly of logic devices intercommunicating by way of a data and address bus, which may not be accessible from outside the assembly. Consequently, the various logic devices, such as memories and other logic functions, cannot be directly tested. The assembly includes a field-programmable gate array (FPGA), which is programmed to perform a particular function during normal operation of the assembly. The FPGA is reconfigured during a test mode of operation into a built-in self-test (BIST) device capable of testing the various logic devices, without requiring significantly more resources on the assembly.

"*Boundary Scan Access of Built-in Self-test for Field Programmable Gate Arrays*" Gibson et al. IEEE International ASIC Conference and Exhibit, Date: 7-10 Sept. 1997 pages 57-61 Inspec Accession Number: 5774208

This paper discusses issues associated with system level access of Built-In Self-Test (BIST) for Field Programmable Gate Arrays (FPGAs) via the Boundary Scan Interface. In addition, we describe the design of an Application Specific Integrated Circuit (ASIC) which serves as an interface between a PC parallel port and the Test

Access Port (TAP) of one or more FPGAs to reprogram the FPGA(s) and administer BIST during off-line testing. There is also included a brief description of the FPGA BIST architecture and operation.

"*Methods for Boundary Scan Access of Built-in Self-test for Field Programmable Gate Arrays*" Hamilton et al. IEEE Southeastcon '99 Proceedings 25-28 March 1999 pages 210 - 216 Inspec Accession Number: 6422210

In this paper are presented four methods for accessing BIST for FPGAs via the IEEE 1149.1 standard boundary scan interface along with the advantages and disadvantages of each approach. Each method is evaluated with consideration to test time, logic overhead, diagnostics resolution, usability in FPGAs, and architectural features which would be required to implement the approach. These methods can be used in a variety of FPGA architectures for all levels of testing.

"*Iterative Improvement Based Multi-way Netlist Partitioning for FPGAs*" Krupnova et al. *This paper appears in:* Design, Automation and Test in Europe Conference and Exhibition Proceedings 9-12 March 1999 pages 587 - 594 Inspec Accession Number: 6390095

This paper presents a multi-way FPGA partitioning method. The basic idea is similar to one proposed by Kuznar et al. (1995), but instead of using the replication and re-optimization, it takes force of the classical iterative improvement partitioning techniques. The basic effort consists in guiding the classical algorithms in their solution

space exploration. This was done by introducing the cost function based on the infeasibility distance of the partitioning solution and carefully tuning the basic parameters of the classical algorithms such as definition of size constraints for feasible moves, handling solutions stack, selecting best cluster to move, etc. The proposed method obtains results comparable to the best published results, and even outperforms them for the largest benchmarks

"*Layout-Driven High Level Synthesis for FPGA Based Architectures*" Xu et al. Design, Automation and Test in Europe Proceedings 23-26 Feb. 1998 pages 446 - 450 Inspec Accession Number: 5906838

This paper addresses the problem of layout-driven scheduling-binding as these steps have a direct relevance on the final performance of the design. The importance of effective and efficient accounting of layout effects is well established in High-Level Synthesis (HLS), since it allows more efficient exploration of the design space and the generation of solutions with predictable metrics. This feature is highly desirable in order to avoid unnecessary iterations through the design process. By producing not only an RTL netlist but also an approximate physical topology of implementation at the chip level, we ensure that the solution will perform at the predicted metric once implemented, thus avoiding unnecessary delays in the design process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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